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Engineered Porous Silicon Counter Electrodes for High Efficiency Dye-Sensitized Solar Cells

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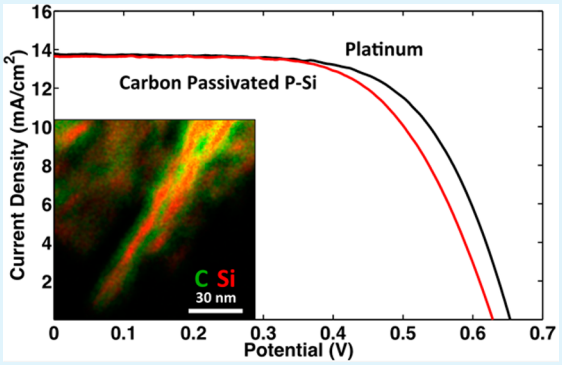
Supporting Information

ABSTRACT: In this work, we demonstrate for the first time, the use of porous silicon (P-Si) as counter electrodes in dye-sensitized solar cells (DSSCs) with efficiencies (5.38%) comparable to that achieved with platinum counter electrodes (5.80%). To activate the P-Si for triiodide reduction, few layer carbon passivation is utilized to enable electrochemical stability of the silicon surface. Our results suggest porous silicon as a promising sustainable and manufacturable alternative to rare metals for electrochemical solar cells, following appropriate surface modification.



KEYWORDS: *dye-sensitized solar cell, counter electrodes, porous silicon, graphene, surface passivation, solar energy conversion*

1. INTRODUCTION

Dye-sensitized solar cells (DSSCs) have emerged as a promising third-generation solar cell due to efficiencies so far measured up to 12%[1−6] and straightforward processes for solar cell manufacturing. A conventional DSSC functions based upon an anode interface between TiO_2 and dye molecules yielding dye photo-oxidation and charge transfer to an iodide/triiodide (I^-/I_3^-) redox couple under illumination. The redox couple is regenerated using a metal counter electrode. Platinum is used as the counter electrode due to its corrosion resistance to iodide species and its excellent electrocatalytic activity toward the iodide/triiodide redox couple.[7−9] However, evolution toward DSSCs that can be cheaply manufactured with low-cost, sustainable materials provides a key incentive toward the development and widespread commercialization of DSSCs.[10]

In recent years, numerous reports have demonstrated the ability to utilize alternative counter electrode materials for DSSCs with performance approaching Pt. This primarily involves the utilization of carbon nanotubes,[11−13] graphene,[14−17] hybrid carbon nanotube−graphene materials,[18,19] and other carbon nanostructures.[20,21] Whereas such approaches yield excellent promise for the use of all-carbon counter electrodes to replace Pt, cell-level integration of such materials is not aided by the high raw-materials cost of carbon nanostructures, which can often be greater than Pt (e.g., > $100/gram), and the requirement to process such raw materials into usable architectures for electrodes that can add significant manufacturing-related costs. Other materials, such as Fe_2O_3 and TiN nanostructures, polymer films, and Cu−Zn−Sn−S have been demonstrated as effective counter electrodes,[22−25] even though challenges regarding stability, efficiency, and conduction properties can be compromised in such alternative systems.

We propose in this study, that silicon is a viable candidate for DSSC electrodes. As the manufacturing of silicon materials is central to electronics and photovoltaics industries, large-scale processing of silicon is cost-effective in comparison to other material options where expensive process development routes are necessary. Furthermore, due to its earth abundance, metallurgical grade silicon materials, which are practical for such applications due to their lower purity requirements than electronics, can be obtained at $2−5/kg. Based purely on raw materials cost, this provides over a 1000× reduction over Pt, if silicon could be a viable electrode material. Whereas the total cost of a DSSC is based on the combined materials and manufacturing costs, silicon is a unique alternative that is promising in both of these areas. Nonetheless, silicon is a material with surface properties strongly influenced by environmental factors, and is highly reactive with ambient air and electrochemical conditions. As a result, in industrial-scale applications where silicon is employed, a critical factor enabling usability is the controlled chemical passivation of exposed silicon surfaces, an area of research which has thrived over the past few decades.[26] In the particular case of porous silicon (P-Si) materials produced from bulk silicon by electrochemical

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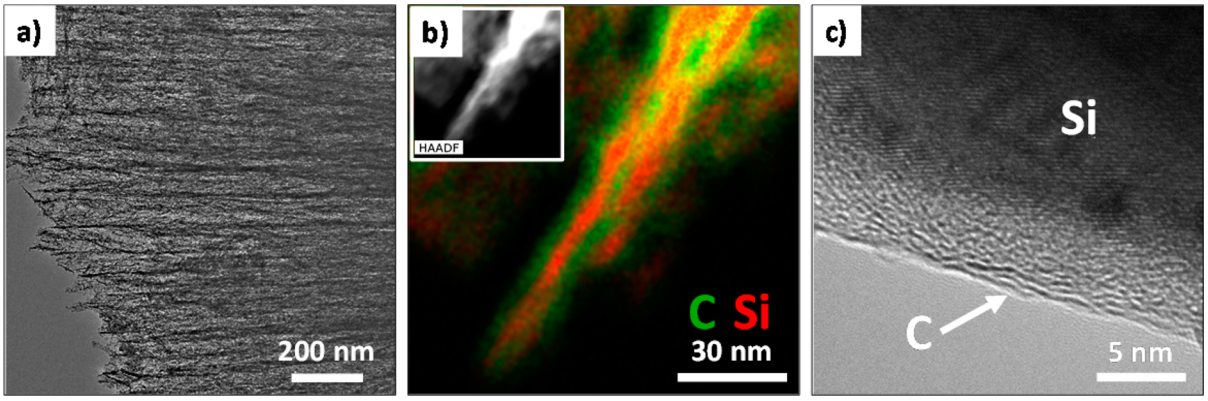

Figure 1. (a) Low resolution TEM image of carbon coated porous silicon. (b) Energy-dispersive spectroscopy map of carbon coated porous silicon with a HAADF STEM image in the inset. (c) High resolution TEM image of few layer graphene on silicon surface.

etching, such routes are especially important due to the significantly enhanced exposed surface area that could potentially provide more catalytically active sites for the I_3^-/I^- redox reaction as a DSSC electrode.[14,19] A variety of routes to passivate the P-Si surface have been described, which can mostly be characterized as involving a Si−O or Si−C surface termination.[27,28] Whereas such routes have been utilized extensively in chemical or biological sensing,[29] controlled surface passivation of P-Si remains unexplored for applications in electrochemical energy conversion platforms.

In this work, we specifically utilize a thermal route to passivate P-Si materials with few-layered coatings of carbon to provide an electrochemically stable DSSC electrode that exhibits performance comparable to Pt. We emphasize the importance of complete silicon surface passivation to enable optimized device performance, and the function of a 3-D porous material to optimize the redox activity. As thermally induced carbon passivation is one of many potential surface stabilization chemistries for silicon, we emphasize silicon as a manufacturable, low-materials cost, and chemically versatile platform for scalable surface modification and replacement of rare metals conventionally employed as DSSC electrodes.

2. EXPERIMENTAL SECTION

TiO_2 Anode Preparation. Anodes were fabricated by first drilling holes in FTO glass (MTI Corp.). FTO glass slides were then sonicated in successive baths of isopropyl alcohol/acetone with 1% Triton-X100 and isopropyl alcohol/acetone for 30 min each, respectively. Glass slides were rinsed with acetone, then isopropyl alcohol, and dried with nitrogen. Glass slides were treated with 40 mM $TiCl_4$ in water for 30 min at 70 °C and then dried in air. A 10 μm thick layer of 20 nm TiO_2 nanoparticles (Dyesol Inc., MS002010) was applied via the doctor blade technique onto the FTO glass using one layer of Scotch tape (3M) to control the thickness of the layer. TiO_2 coated anodes were annealed at 500 °C for 30 min in air followed by another 40 mM $TiCl_4$ treatment for 12 h at 35 °C. This treatment is crucial to cell performance as a TiO_2 sol gel is formed and fills gaps in the mesoporous TiO_2 nanoparticle layer preventing recombination of e^-/h^+ pairs. A scattering layer composed of 300 nm TiO_2 nanoparticles (Dyesol Inc., MS002260) is added on top of the active layer and annealed at 500 °C. Finally, anodes were immersed in 0.6 mM *cis*-bis(isothiocyanato) bis(2,2′-bipyridyl-4,4′-dicarboxylato)ruthenium-(II) (N-719 Dye) in ethanol overnight (Sigma, 703206).

C-Passivation of Porous Silicon. Highly boron-doped (0.01−0.2 Ωcm) silicon wafers (University Wafer) were etched in an electrochemical cell using a spiral Pt counter electrode according to our previously published procedure.[30] A 180 s etch process was utilized with a current density of 45 mA/cm^2 in a 3:8 v/v HF (50% H_2O by volume) and ethanol solution. This produces porous silicon materials with ∼75% porosity, confirmed by optical reflectometry, and an average pore size just under 25 nm.[31] Porous silicon was stored under N_2 until carbonization. For C-passivation, a porous silicon wafer was placed into a tube furnace at room temperature and the furnace was evacuated to 2 mTorr. Next, 1000 sccm of Ar and 200 sccm of H_2 were introduced to the system and the furnace was ramped to T_1. T_1 was equal to 550, 650, and 750 °C for the three different C-passivated P-Si samples, respectively. The purpose of the H_2 is to maintain a reducing environment that preserves the surface stability of the unpassivated porous silicon from oxidation. Acetylene was introduced and the temperature was ramped to T_1 + 100. Ten minutes after C_2H_2 introduction, the temperature was ramped to T_1 + 150 for 10 min. This process was chosen because our observations in preliminary experiments demonstrated (i) porous silicon is not thermally stable without passivation above 750 °C, (ii) carbon coating thermally stabilizes the porous silicon up to ∼1000 °C or higher, and (iii) the best "quality" of carbon materials based on Raman spectroscopy analysis were formed in the temperature range between 550 and 850 °C. Therefore, these conditions are able to optimize both the reactivity of the silicon for coating, the quality of carbon material, and the preservation of the nanoscale structure of the porous silicon after treatment. Following the second 10 min step, C_2H_2 flow was discontinued and the sample was allowed to cool to 50 °C in an Ar and H_2 atmosphere. Samples were stored in an N_2 atmosphere until use to prevent oxidation.

DSSC Fabrication. Platinum cathodes were prepared by brushing 25 mM H_2PtCl_6 (Sigma 254029) in isopropyl alcohol onto clean FTO glass substrates. Samples were then calcined at 450 °C for 1 h. The cathode and anode were heat sealed with Surlyn film (McMaster Carr, 7622A41) and filled with the electrolyte composed of 50 mM I_2, 500 mM LiI, and 500 mM tertbuylpyridine (TBP) in acetonitrile, and heat sealed.

Electrochemical Testing. Dye-sensitized solar cells were tested over a potential range of −1 to +1 V at a scan rate of 50 mV/s under AM 1.5 illumination (100 mW/cm^2) with a Newport solar simulator and power supply. An area of 0.12 cm^2 was illuminated; the remainder was covered with a shadow mask. Cyclic voltammetry (CV) measurements were carried out in a three-electrode setup using nitrogen bubbled acetonitrile which contained 0.1 M $LiClO_4$, 10 mM LiI, and 1 mM I_2 as an electrolyte over a potential range of +1 to −0.8 V. A Pt foil was used as the counter electrode, and Ag/AgCl was used as a reference electrode. Electrochemical impedance spectroscopy measurements were performed over a frequency range of 10^{-1} to 10^5 Hz. A MetroOhm PGSTAT101 potentiostat was used for all electrochemical measurements.

Material Characterization. An FEI Osiris transmission electron microscope was used with an accelerating voltage of 200 kV for all transmission electron microscopy (TEM) imaging. Raman spectra were gathered using a 532 nm DPSS laser in which the output power was limited to 10% (maximum output power 50 mW). The Raman

scattered photons were dispersed by a 1200 lines/mm grating monochromator and collected by a CCD camera with a 50× objective lens.

3. RESULTS AND DISCUSSION

Thermal passivation of P-Si materials was achieved, consistent with our previous studies,[30] and building from efforts by Salonen et al.[32,33] This involves exposure of P-Si to an environment containing a diluted C_2H_2 active species (<0.1%) in H_2/Ar. To achieve full passivation and maintain structural integrity of the P-Si nanoscale features, we observed the passivation temperature to be important. Prolonged exposure to temperatures greater than 750 °C led to irreversible structural changes to the P-Si, which were alleviated by introducing temperature ramps from below 750 °C to temperatures above this, as the formation of a thin carbon coating passivated the surface from thermal degradation at high temperatures. As discussed at a later point, our most ideal temperature ramp condition was obtained between 650 and 800 °C, which enabled complete catalytic surface passivation without thermal decomposition of the C_2H_2 species that was found to yield low-quality carbon materials. Whereas we chose thermal passivation for our work, progress in silicon surface passivation using wet chemical approaches, such as surface alkylation,[34,35] could ultimately enable a similar outcome to the results we discuss here.

The morphology of the carbon coated porous silicon is shown via low resolution TEM (Figure 1a). To confirm and assess the presence of carbon on the silicon surface after thermal passivation, a high angle annular dark field (HAADF) image was obtained with energy-dispersive X-ray spectroscopy (EDS) mapping of carbon and silicon (Figure 1b); the corresponding spectrum is in the Supporting Information (Figure S1). A high resolution TEM image showing the carbon−silicon interface and presence of few-layer carbon coatings is presented in Figure 1c. To assess the carbon material properties, fast Fourier transform analysis was used to determine the interlayer spacing, which was found to be between 0.35 and 0.37 nm (Supporting Information, Figure S2). This spacing represents a graphene material with interlayer defects; it is greater than pristine defect-free graphene (~0.34 nm)[36,37] but lower than most forms of chemically processed graphene, such as reduced graphene oxide (often >0.4 nm).[38] Therefore, we emphasize under these conditions, that the thermal surface passivation of P-Si leads to a uniform, few-nanometer thick coating of conformal graphene layers catalyzed by the nanoscale silicon material.

DSSCs with C-passivated porous silicon counter electrodes were designed by depositing a TiO_2 active layer adsorbed with Di-tetrabutylammonium *cis*-bis(isothiocyanato)bis(2,2′-bipyridyl-4,4′-dicarboxylato)ruthenium(II) (N719) dye on the fluorine tin oxide (FTO) glass followed by a TiO_2 scattering layer. A liquid electrolyte consisting of the I^-/I_3^- redox couple was utilized for electron transport between the electrodes. A schematic representation of a typical DSSC made with C-passivated porous silicon is illustrated in Figure 2a and the front and back views of the counter electrode are shown in Figure 2b.

The characteristics of the P-Si surface passivation are observed to directly correlate with DSSC performance. To study the effect of C-passivation on the catalytic properties of porous silicon, DSSCs were fabricated with pristine P-Si and thermal passivation at three different temperature ramp profiles including 550−700, 650−800, and 750−900 °C (details in the

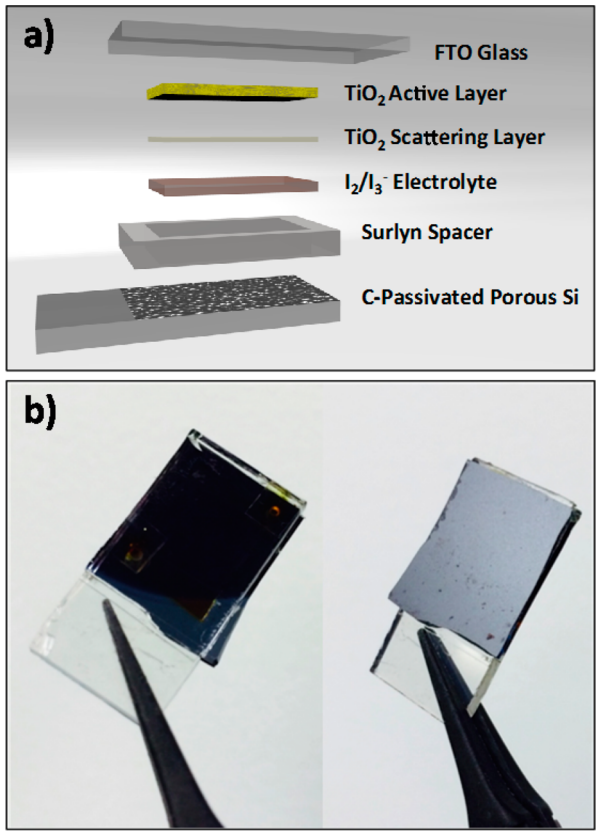

Figure 2. (a) Schematic of dye-sensitized solar cells fabricated with C-passivated porous silicon counter electrode. (b) Front (left) and back (right) view of DSSC with C-passivated porous silicon counter electrode.

Experimental Section). The C-passivation layer was characterized by acquiring Raman spectra for all four samples (Figure 3a). Pristine P-Si has a single strong peak near 520 cm^{-1}, indicative of silicon. After thermal passivation, two distinctive peaks arise at 1325 cm^{-1} (D-band) and 1602 cm^{-1} (G-band) that are characteristic of graphitic carbon coatings.[39] The D/G peak height is indicative of the ratio of sp^3 to sp^2 hybridized carbon species, which is notably consistent at D:G = 0.76 until the highest temperature conditions (750−900 °C), where D:G is 1.22. We attribute this to a decrease in crystallinity of the C-passivation layer associated with higher temperature non-catalytic decomposition of C_2H_2 species. Notably, we do not observe the presence of a significant oxide layer on the silicon, which is evident in the Raman spectra through a bump near 800 cm^{-1}. To better understand the properties of C-passivation, we measured conductance through the P-Si layer in the different C-passivated P-Si materials. It is known that P-Si materials exhibit defect-induced surface traps that can reverse the effect of chemical doping and decrease the P-Si conductance by several orders of magnitude.[40] Measurements were carried out by sandwiching porous silicon electrodes between two plates connected with copper wires, and performing I−V curves (Supporting Information). This forces the porous silicon layer to be a resistive component in series with the bulk silicon, enabling us to assess the effect of surface passivation on the porous silicon electrical properties. We find the conductance to increase between 3 and 5 orders of magnitude through C-passivation, calculated over the ohmic region from current−voltage scans shown in Figure 3b. This

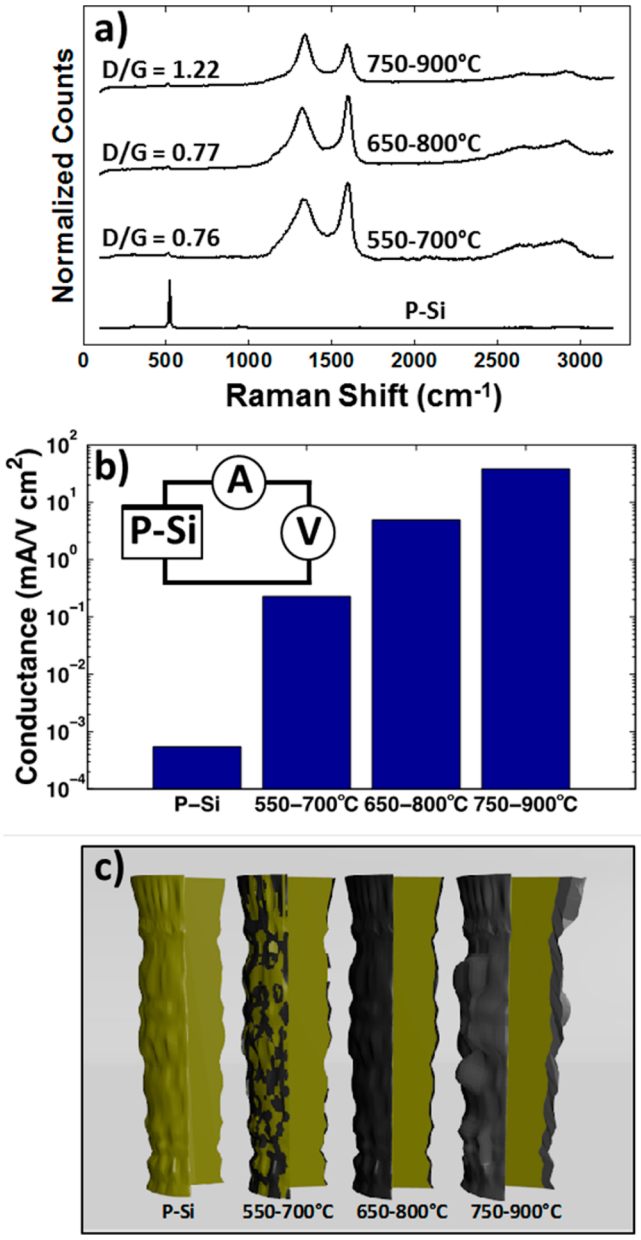

Figure 3. (a) Raman spectra of pristine porous silicon and porous silicon C-passivated at different temperatures, peaks are normalized to the 1602 cm^{-1} G-peak. (b) Calculated conductance values for porous silicon and C-passivated porous silicon at different temperatures with (inset) schematic of through plane measurement setup. (c) Schematic representation of carbon coating (black) on a section of porous silicon (yellow) for each sample type. The coating coverage and thickness were determined using data from cyclic voltammetry, electrochemical impedance spectroscopy, and through plane conductivity. The structure on the right is shaded differently to indicate the higher ratio of sp^3 to sp^2 carbon.

observation is complemented by two additional observations: (i) post C-passivation Si etch experiments in KOH led to small, polydispersed flakes at 550−700 °C and coherent films at 650−800 °C (Supporting Information, Figure S4) and (ii) TEM imaging of C-passivated regions did not show a distinct layer thickness dependence between the different C-passivation temperatures. We do not anticipate that the formation of an oxide layer would affect this result because we observe no presence of an oxide layer in these materials (Raman and TEM analysis), and any effect of an oxide layer on the conductivity would be consistent across all samples. This leads us to conclude that (i) ramp conditions with terminal temperatures below 700 °C lead to incomplete surface passivation, in turn leading to exposed Si surface, (ii) ramp conditions from 650 to 800 °C lead to ideal surface passivation, and (iii) terminal temperatures in ramp conditions of 900 °C and above lead to thicker, less crystalline carbon passivation layers (Figure 3c).

DSSCs were constructed with the C-passivated porous silicon fabricated at the three conditions and compared to reference DSSCs constructed with standard Pt counter electrodes. Photocurrent spectra of DSSCs under AM 1.5 illumination are shown in Figure 4a. The short circuit current density (J_{sc}), open circuit voltage (V_{oc}), calculated efficiency, and fill factor (FF) are summarized in Table 1. DSSCs with a P-Si counter electrode exhibited an efficiency of 0.21% relative to an efficiency of 5.80% for the platinized FTO counter electrodes, which we can attribute to either the poor electrochemical stability native to unpassivated silicon that drives corrosion, the lack of conductivity (Figure 3b), or the lack of catalytically active sites for triiodide reduction that are developed through surface modification. DSSCs made with 650−800 °C C-passivated P-Si exhibited an efficiency of 5.38%, which is comparable to that of solar cells constructed using Pt counter electrodes. Comparatively, DSSCs constructed with C-passivation conditions of 550−700 °C and 750−900 °C exhibited efficiencies of 2.13% and 3.95%, respectively. This indicates C-passivation at temperatures of 650−800 °C leads to ideal performance that seems to correlate with previous material charge-transport analysis shown in Figure 3. We also note that DSSCs fabricated with C-passivation at 750−900 °C had a relatively good efficiency and fill factor compared to P-Si and those constructed at 550−700 °C. This can be attributed to the full coverage and passivation of porous silicon by carbon which minimizes the charge recombination on the surface and lowers the charge transfer resistance. Long-term illumination studies of the passivated P-Si counter electrodes in comparison to Pt (Supporting Information, Figure S7) emphasize the ability for the passivation layer to enable long-term operation of this electrode material.

To understand these inherent differences in performance, the C-passivated P-Si counter electrodes were characterized with electrochemical impedance spectroscopy (EIS), and cyclic voltammetry. EIS was performed on symmetric counter electrode cells over a frequency range of 10^{-1} to 10^5 Hz in order to investigate the charge transfer properties in the system (Figure 4b). The first semicircle is representative of the charge transfer resistance and double layer capacitance at the cathode. The second, low frequency semicircle is indicative of electrolyte diffusion between electrodes. The observed differences in the impedance between the DSSCs constructed with the Pt counter electrode and the C-passivated P-Si at 650−800 °C (Figure 4b) are attributed to a combination of (i) higher resistance to electron transfer, stemming from the insulating porous silicon interface between the carbon coating and conductive silicon substrate and (ii) slower ionic diffusion, likely due to the poor reduction of triiodide species at the C-passivated P-Si relative to the planar Pt. To further elucidate these mechanisms, an appropriate equivalent circuit model was fit to the system[41] provided in the inset of Figure 4b. Series (R_s) and charge transfer (R_{ct}) resistances were calculated from the circuit model shown in Figure 4c. The model reveals that the series and charge transfer resistances of both pristine P-Si and C-

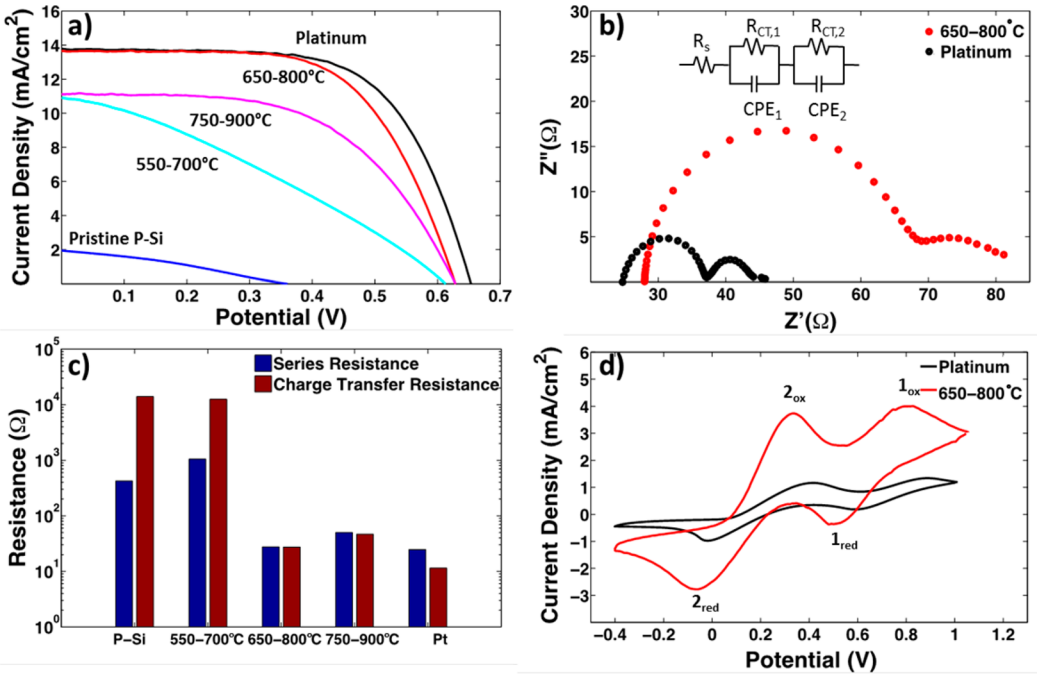

Figure 4. (a) J−V curves of DSSCs designed with the C-passivated porous silicon fabricated at different temperatures under AM 1.5 G illumination. The J−V curve of the Pt counter electrode is included as well. (b) Nyquist plots of symmetric cells made from carbon coated porous silicon and platinum under zero voltage bias over a frequency range of 10^{-1} to 10^{5} Hz with equivalent circuit diagram provided (inset). Here CPE refers to constant phase element, R_{ct} refers to charge transfer resistance, and R_S refers to series resistance. (c) Calculated series and charge transfer resistances of different counter electrodes measured over identical P−Si sample areas of 0.12 cm^2. (d) Cyclic voltammograms of carbon coated porous silicon fabricated at 650−800 °C and Pt. Reaction 1 refers to $3I_2 + 2e^- \rightarrow 2I_3^-$ and reaction 2 refers to $I_3^- + 2e^- \rightarrow 3I^-$, the latter occurring at the counter electrode.

Table 1. Efficiencies, Fill Factors, Short Circuit Currents and Open Circuit Voltages of All Devices

counter electrode	efficiency (%)	FF (%)	J_{sc} (mA/cm^2)	V_{oc} (V)
P-Si	0.21	31.5	1.94	−0.36
550−700 °C	2.13	31.8	10.9	−0.61
650−800 °C	5.38	62.4	13.7	−0.63
750−900 °C	3.85	56.6	11.1	−0.63
Pt	5.80	64.4	13.8	−0.65

passivated P-Si thermally treated at 550−700 °C are orders of magnitude higher than the corresponding resistances of samples treated at 650−800, 750−900 °C, and Pt. The magnitude of the resistances found with P-Si and the 550−700 °C sample is attributed to corrosion occurring on exposed Si surface.[34,35] Series resistance varies with C-passivation thickness,[38,39] and is lowest for the platinum sample, increases for the 650−800 °C sample and 750−900 °C sample.[42,43] It should be noted that this is qualitatively in agreement with through-plane conductivity measurements (Figure 3b), even though this value of R_s is more relevant to the electrode-limited resistance of the full device with the porous silicon−electrolyte interface. The lower R_{ct} of Pt is a result of less recombination at the cathode relative to C-passivated P-Si, and hence slightly faster kinetics of triiodide reduction that is indicative of an efficient counter electrode material. The 750−900 °C treated P-Si sample has a higher R_{ct} than the 650−800 °C treated samples due to its reduced ability for triiodide reduction, a result of its highly defective carbon coating. These effects enhance the interfacial charge transfer events, lower the overall resistance, and augment the efficiencies and fill factor. For the sake of clarity, Nyquist plots of only Pt counter electrodes and C-passivated P-Si thermally treated at 650−800 °C are shown in Figure 4b; Nyquist plots for other counter electrodes are provided in the Supporting Information (Figure S5).

To further understand the electrochemical properties of the different C-passivated porous silicon samples, cyclic voltammetry (CV) measurements were carried out in a three-electrode setup, as detailed in the Supporting Information. The CV curve of the Pt counter electrode (Figure 4d) is similar to that found in the literature.[44] Two sets of peaks were observed, corresponding to the reduction of iodine to triiodide given by redox reactions 1 and reduction of triiodide to iodide ions given by reaction 2

$$3I_2 + 2e^- \rightarrow 2I_3^- \quad (1)$$

$$I_3^- + 2e^- \rightarrow 3I^- \quad (2)$$

The separation of the reduction and oxidation peaks, E_{pp}, is indicative of the electrochemical catalytic activity of the counter electrodes, which is independent of their surface area.[14,45] Values for E_{pp} of 0.40 and 0.43 V were found for the samples passivated at 650−800 °C and Pt, respectively, which indicates that the catalytic ability of C-passivated P-Si for the I^-/I_3^- redox couple is on par with Pt. Porous-Si samples passivated at 750−900 °C exhibited an E_{pp} value of 0.54, indicating that the surface passivation at the higher temperatures is not as effective of a catalyst, due to the high defect ratio.[46] Due to the high surface area of porous silicon, the redox peaks are much larger for the C-passivated P-Si than for the planar Pt, which explains the comparable efficiencies of the DSSCs. CV measurements of both P-Si and the C-passivated samples at 550−700 °C (Supporting Information, Figure S6) show their poor catalytic activity for I^-/I_3^- oxidation reaction. The incomplete

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passivation achieved at 550−700 °C likely gives rise to high charge recombination on the exposed Si and inadequate redox chemistries resulting in low efficiency and poor fill factor. We note that we also performed a control experiment using planar silicon as a counter electrode for DSSC (Supporting Information, Figure S7) and did not observe a measurable photocurrent.

Overall, whereas we emphasize in this work that passivated Si materials are viable candidates for the replacement of Pt in DSSCs, our results indicate a synergistic codependence of the passivation layer and silicon material properties that dictates overall behavior. In regimes of incomplete passivation, poor device performance is indicative of poor charge-transport properties and a high R_{ct} that inhibits redox activity. However, in regimes of complete passivation with poor quality coatings, inefficient redox activity inhibits performance matching that of Pt reference cells. The benefit of silicon in such a material platform is the tunable surface chemistry between the silicon and carbon that can enable optimal performance as a counter electrode in a DSSC. Whereas we demonstrate this to be a viable platform that can be utilized in the context of an on-chip system, we emphasize the versatility of this technique's scale to a diverse scope of microscale and nanoscale silicon heterogeneous materials that can provide a new, sustainable alternative material for efficient DSSC fabrication. In comparison to other solar energy conversion systems using silicon, where processing and interface optimization are necessary to enable efficient device performance, we demonstrate heterogeneous porous silicon materials that natively exhibit the capability to be electrodes for DSSCs with appropriate surface modification.

4. CONCLUSIONS

Although our specific work is focused on thermally applied carbon passivation layers resembling graphene, the use of silicon reflects a versatile chemical platform for optimizing the electrode−electrolyte interface in a DSSC using scalable routes such as wet-chemical, thermal, and electrochemical passivation. Compared to other homogeneous materials employed as counter electrodes in DSSCs, this approach represents the utilization of a heterogeneous material interface that we propose provides enhanced flexibility in achieving scalable device optimization. As silicon exists in nearly all applications as a heterogeneous material in some form, and these applications represent the majority of our current technological infrastructure, we see this approach as directly building upon a material platform already integrated into scalable industrial manufacturing processes. Furthermore, as DSSCs involve a native low-cost cell design with promise for versatility and cost that could ultimately replace silicon photovoltaics, we emphasize the fascinating notion of silicon to empower such a transition for DSSCs. As raw material costs of silicon are only a minor portion of commercial PV costs, the low-cost assembly of Si-based DSSCs to replace conventional PV platforms could build upon, instead of compete with, aggressive worldwide government−corporate investments aimed to improve silicon manufacturing for solar applications.

■ ASSOCIATED CONTENT

Supporting Information

EDS spectrum corresponding to Figure 1b, TEM and FFT of graphene oxide with d-spacing of 0.35−0.36 nm, through plane conductivity measurements over the potential range of −100mV to +100mV for each porous silicon sample used, through plane conductivity schematic, image of the carbon coating when silicon has been dissolved away via KOH etching, Nyquist plots and corresponding modeled data for symmetric cells, cyclic voltammograms of all samples carried out in a three-electrode setup using nitrogen bubbled acetonitrile, and stability tests of DSSCs with Pt and C-passivated P-Si counter electrodes over 2 h. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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